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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
GUILL, RUSSELL L	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,007	WHEELER ET AL.	
	Examiner	Art Unit	
	Russ Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 15-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15-29 and 32* is/are rejected.

7)☒ Claim(s) *30,31 and 33-37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to an Amendment filed July 13, 2006. Claim 14 has been cancelled. Claims 1 – 13 and 15 – 37 are pending. Claims 1 – 13 and 15 – 37 have been examined. **Claims 30 - 31 and 33 – 37 are objected to as being dependent upon a rejected base claim**. Claims 1 – 13, 15 – 29 and 32 have been rejected.

2. This Office Action is NON-final due to especially relevant new art that was located during an updated search.

3. **The Examiner would like to thank the Applicant for the well-presented response, which assisted in the examination process**. The Examiner appreciates the effort to thoroughly analyze the Office Action and make appropriate arguments and amendments.

Response to Remarks

4. Regarding claims 1, 7 – 8, 10 – 11, 25 – 29, 30 – 31 and 35 – 37 rejected under 35 USC § 101:

   4.1. Applicant's amendments to the claims overcome the rejections. The Examiner remarks that a tangible (i.e. real world) result may also flow inherently from a claim.

5. Regarding claims 1 and 13 rejected under 35 USC § 102 (Bargh) and 35 USC § 102 (Watkins):

   5.1. Applicant's arguments have been fully considered, and are persuasive. Accordingly, the rejections are withdrawn. However, upon further consideration a new rejection is made using new art located during an updated search.

6. Regarding claim 25 rejected under 35 USC § 102 (Watkins):

6.1. Applicant's arguments have been fully considered and are persuasive. Accordingly, the rejections are withdrawn.

7. Regarding claim 25 rejected under 35 USC § 102 (Bargh):

7.1. Applicant's arguments have been fully considered, but were not found to be persuasive, as follows.

7.2. The Applicant argues:

7.2.1. As described above, simulation model of Bargh discloses "design entities" and "instrumentation entities", which are distinct entities and the instrumentation entity of Bargh does not appear to be integrated with the logic design element to automatically collect instrumentation data relating to the logic design. The block 420 of Fig. 4B appears to be an instrumentation logic block 420 to record occurrences of each type of events of each design entity. The instrumentation logic block 420 appears to be a common space to record the events of each design entity. As depicted in Fig. 4B, the instrumentation logic block 420 appears to be recording the occurrence of events of the instantiations 321a, 321b and 322.

7.2.1.1. The Examiner respectfully replies:

7.2.1.1.1. The Applicant recites on page 13, section Claims 1 and 13, "However, Bargh indicates that design entity is monitored by the instrumentation entity without the instrumentation entity becoming incorporated into the digital design circuit. Bargh discloses (. . .) a simulation model comprising 'design entities' and 'instrumentation entities'. An instrumentation entity is associated with a design entity referred to as a target entity. Instances of instrumentation entities are created and *connected to the target entities within the simulation model* (emphasis added by Examiner).

However, the instrumentation entity and target entity are two distinct entities and the instrumentation entity is not incorporated into the design entity." The Applicant appears to indicate that the instrumentation entity is connected to the design entity, which certainly qualifies as being integrated with the logic design element. Further, Bargh recites in column 12, lines 50 – 56, "A body section 402 of the instrumentation entity 409, contains logic necessary to detect occurrences of certain "events" on signals 401 of the target entity". This appears to indicate that the instrumentation entity is more than just a common space of counters, but also includes logic. Bargh also recites in column 13, lines 20 – 25, "Count events are utilized to monitor the frequency of occurrence of specific sequences within a simulation model", which is certainly collecting usage and performance statistics. Accordingly, the rejection is maintained.

8. Regarding claims 7 – 9 and 19 - 21 rejected under 35 USC § 103 (Watkins/Sharma):

8.1. Applicant's arguments have been fully considered and are persuasive. However, upon further consideration, a new rejection is made.

9. Regarding claims 10 - 12 and 22 - 24 rejected under 35 USC § 103 (Watkins/Mitchell):

9.1. Applicant's arguments have been fully considered and are persuasive.

10. Regarding claim 30 rejected under 35 USC § 103 (Watkins/Wong):

10.1. Applicant's arguments have been fully considered and are persuasive.

11. Regarding claim 32 rejected under 35 USC § 103 (Watkins/Srivastava):

11.1. Applicant's argument has been fully considered, but is not persuasive, as follows.

11.2. In summary, the Applicant argues that Srivastava does not teach a tri-state bus.

11.3. The Examiner respectfully replies: The Examiner agrees, however, Srivastava appears to teach a FIFO, which appears to overcome the argument.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claim 25 is rejected under 35 U.S.C. 102(e) as being anticipated by Bargh (U.S. Patent 6,195,627).

13.1. Regarding **claim 25**:

13.1.1. Bargh appears to teach a simulation module that is structured and arranged to perform a simulation of a logic design that includes a logic design element (***Abstract, and columns 7 – 8, and figures 3A and 3B***).

13.1.2. Bargh appears to teach a collection module that is integrated with the logic design element and that is structured and arranged to automatically collect and store instrumentation data, which represents usage and performance related statistics

relating to the logic design element during the simulation (***figure 4B, element 420; and column 12, lines 25 - 67, and columns 13 - 14***).

13.1.3. Bargh appears to teach a processor (***figure 2, element 24***).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

16. Claims 1 - 2 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bargh (U.S. Patent 6,195,627), in view of Schubert (U.S. Patent Number 6,581,191).

16.1. Regarding **claim 1**:

16.2. Bargh appears to teach:

16.2.1. using a logic design element in a logic design (**Abstract**);

16.2.2. performing a simulation of the logic design that includes simulating the logic design element (**Abstract**);

16.2.3. automatically collect and store instrumentation data during the simulation (**figures 4A and 4B, especially elements 421, 422, 423, 424; and column 12, lines 25 – 67, and columns 13 – 14**);

16.2.4. instrumentation data represents usage and performance related statistics that relate to the logic design element (**figures 4A and 4B, especially elements 421, 422, 423, 424; and column 12, lines 25 – 67, and columns 13 – 14**);

16.3. Bargh does not specifically teach:

16.3.1. having the logic design element automatically collect and store instrumentation data during the simulation.

16.4. Schubert appears to teach:

16.4.1. having the logic design element automatically collect instrumentation data during the simulation (**figures 1A, 1B, 2; and column 13, lines 43 – 67, and column 14, lines 1 – 23; and column 12, lines 20 – 30; *Please note that in column 12, lines 20 – 30, the DUT itself is a logic design element being typically part of a larger hardware product***).

16.5. The motivation to use the art of Schubert with the art of Bargh would have been the benefits recited in Schubert, including the customized DIC (Design Instrumentation

Circuitry) makes efficient use of its circuitry, and since the DIC consumes area on the hardware product, making the customized DIC efficient and compact is advantageous (**column 15, lines 60 – 67**).

16.6. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Schubert with the art of Bargh to produce the claimed invention.

16.7. Regarding **claim 2**:

16.8. Bargh appears to teach:

16.8.1. displaying the instrumentation data relating to the logic design element (**column 1, lines 61 – 67, and column 2, lines 1 – 2; and figure 1, element 22**);

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16.9. Regarding **claim 13**:

16.10. Bargh appears to teach:

16.10.1. using a logic design element in a logic design (**Abstract**);

16.10.2. performing a simulation of the logic design that includes simulating the logic design element (**Abstract**);

16.10.3. automatically collect instrumentation data during the simulation (**figures 4A and 4B, especially elements 421, 422, 423, 424; and column 12, lines 25 – 67, and columns 13 – 14**);

16.10.4. instrumentation data represents usage and performance related statistics that relate to the logic design element (**figures 4A and 4B, especially elements 421, 422, 423, 424; and column 12, lines 25 – 67, and columns 13 – 14**);

16.10.5. displaying the instrumentation data relating to the logic design element (**column 1, lines 61 – 67, and column 2, lines 1 – 2; and figure 1, element 22**);

16.11. Bargh does not specifically teach:

16.11.1. having the logic design element automatically collect and store instrumentation data during the simulation.

16.12. Schubert appears to teach:

16.12.1. having the logic design element automatically collect instrumentation data during the simulation (**figures 1A, 1B, 2; and column 13, lines 43 – 67, and column 14, lines 1 – 23; and column 12, lines 20 – 30; *Please note that in column 12, lines 20 – 30, the DUT itself is a logic design element being typically part of a larger hardware product***).

17. Claims 3 - 6 and 15 - 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bargh as modified by Schubert as applied to claims 1 - 2 and 13 above, further in view of Watkins (U.S. Patent 5,220,512).

17.1. Bargh as modified by Schubert teaches a method of simulating a logic design as recited in claims 1 - 2 and 13 above.

17.2. Regarding claims 3 and 15:

17.2.1. Watkins appears to teach receiving a query to display the instrumentation data relating to the logic design element, wherein displaying the instrumentation data relating to the logic design element in response to the query (***column 6, lines 45 – 53***).

17.2.1.1. Regarding (***column 6, lines 45 – 53***); attaching a data area that displays state data is a query.

17.3. The motivation to use the art of Watkins with the art of Bargh as modified by Schubert would have been the benefit recited in Watkins that the invention provides an improved ECAD system whereby the characteristics of the schematic editor, schematic compiler, and simulator are all presented to the user in a fashion such that they appear as a single integrated function (**column 4, lines 50 – 56**).

17.4. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Watkins with the art of Bargh as modified by Schubert to produce the claimed invention.

17.5. Regarding claims 4 and 16:

17.5.1. Watkins appears to teach displaying the instrumentation data after performing the simulation (***column 5, lines 14 – 16***).

17.6. Regarding claims 5 and 17:

17.6.1. Watkins appears to teach displaying the instrumentation data while performing the simulation (***column 7, lines 48 – 57***).

17.7. Regarding claims 6 and 18:

17.7.1. Watkins appears to teach performing the simulation means performing a partial simulation (***column 7, lines 12 – 27***).

17.7.2. Watkins appears to teach having the logic design element automatically collect the instrumentation data during the partial simulation (***column 7, lines 24 – 27***).

17.7.3. Watkins appears to teach displaying the instrumentation data includes displaying the instrumentation data after performing the partial simulation (***column 7, lines 12 – 27***).

18. Claims 7 – 9 and 19 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bargh as modified by Schubert as applied to claims 1 - 2 and 13 above, further in view of Srivastava (Mani B. Srivastava et al; "Using VHDL for High-Level, Mixed –Mode System Simulation", September 1992, IEEE Design & Test of Computers, Volume 9, Issue 3).

18.1. Bargh as modified by Schubert teaches a method of simulating a logic design as recited in claims 1 - 2 and 13 above.

18.2. Regarding **claims 7 and 19**:

18.3. Bargh as modified by Schubert appears to teach:

18.3.1. wherein having the logic design element automatically collect the instrumentation data includes automatically collect the instrumentation data during the simulation (**please refer to claims 1 and 13**).

18.4. Bargh as modified by Schubert does not specifically teach:

18.4.1. the logic design element includes a FIFO;

18.4.2. having the logic design element automatically collect the instrumentation data includes having ***the FIFO memory*** automatically collect the instrumentation data during the simulation, with ***the instrumentation data relating to the FIFO memory***.

18.5. Srivastava appears to teach:

18.5.1. the logic design element includes a FIFO (***page 36, figure 3, message buffer***).

18.5.2. the instrumentation data relates to the FIFO memory (***page 36, figure 3, message buffer and statistics***).

18.6. The motivation to use the art of Srivastava with the art of Bargh is the advantages recited in Srivastava that VHDL enables simulation across many different levels of abstraction (***page 31, last sentence, and page 32, first two sentences***). This advantage would have been recognized by the ordinary artisan as a benefit.

18.7. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Srivastava with the art of Bargh to produce the claimed invention.

18.8. Regarding **claims 8 and 20**:

18.9. Bargh as modified by Schubert does not specifically teach:

18.9.1. having the FIFO memory record usage of the FIFO memory during the simulation.

18.10. Srivastava appears to teach:

18.10.1. having the FIFO memory record usage of the FIFO memory during the simulation (***page 36, figure 3, message buffer***).

18.11. Regarding **claims 9 and 21**:

18.12. Bargh as modified by Schubert appears to teach:

18.12.1. receiving a query to display the instrumentation data (**column 1, lines 61 - 67, and column 2, lines 1 - 2; and figure 1, element 22**);

18.12.2. displaying the instrumentation data in response to the query (**column 1, lines 61 - 67, and column 2, lines 1 - 2; and figure 1, element 22**).

18.13. Bargh as modified by Schubert does not specifically teach:

18.13.1. receiving a query to display the instrumentation data ***relating to the FIFO memory***;

18.13.2. displaying the instrumentation data ***relating to the FIFO memory*** in response to the query.

18.14. Srivastava appears to teach:

18.14.1. instrumentation data relating to the FIFO memory (***page 36, figure 3, message buffer***).

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19. Claims 10 - 12 and 22 - 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bargh as modified by Schubert as applied to claims 1 - 2 and 13 above, further in view of Koseko (Yasushi Koseko; "Tri-state bus conflict checking method for ATPG using BDD",

1993, Proceedings of the 1993 IEEE/ACM International conference on Computer-aided design, pages 512-515).

19.1. Bargh as modified by Schubert teaches a method of simulating a logic design as recited in claims 1 - 2 and 13 above.

19.2. The art of Koseko is directed toward tri-state bus conflict checking (***Title***).

19.3. Regarding **claims 10 and 22**:

19.3.1. Bargh as modified by Schubert appears to teach that having the logic element automatically collect the instrumentation data includes having the logic element automatically collect the instrumentation data during the simulation, with the instrumentation data relating to the logic element (***Please refer to claims 1 and 13***).

19.3.2. Bargh as modified by Schubert does not specifically teach that ***the logic design element includes a tri-state bus***.

19.3.3. Bargh as modified by Schubert does not specifically teach having the logic element automatically collect the instrumentation data includes having the ***tri-state bus*** automatically collect the instrumentation data during the simulation, with the instrumentation data relating to the ***tri-state bus***.

19.3.4. Koseko appears to teach that a logic design includes a tri-state bus (***Page 512, section 1 Introduction, and figure 1***).

19.3.5. The motivation to use the art of Koseko with the art of Bargh is the benefit recited in Koseko that the method is a practical bus design rule checking method that avoids wasteful work avoids wasteful work (**page 512, section 1. Introduction, right-side column, third paragraph**).

19.4. Regarding **claims 11 and 23**:

19.4.1. Bargh as modified by Schubert appears to teach that having a logic element automatically collect the instrumentation data includes having a logic element automatically collect usage of a logic element during the simulation (***Please refer to claims 1 and 13***).

19.4.2. Bargh as modified by Schubert does not specifically teach that having the ***tri-state bus*** automatically collect the instrumentation data includes having the ***tri-state bus*** automatically collect usage of the ***tri-state bus*** during the simulation.

19.4.3. Koseko appears to teach a logic design that includes a tri-state bus (***Page 512, section 1 Introduction, and figure 1***).

19.5. Regarding **claims 12 and 24**:

19.5.1. Bargh as modified by Schubert appears to teach receiving a query to display the instrumentation data relating to a logic element (***column 1, lines 61 – 67, and column 2, lines 1 - 2; and figue 1, element 22***).

19.5.2. Bargh as modified by Schubert appears to teach displaying the instrumentation data relating to a logic element in response to the query (***column 1, lines 61 – 67, and column 2, lines 1- 2; and figue 1, element 22***).

19.5.3. Bargh as modified by Schubert does not specifically teach receiving a query to display the instrumentation data relating to the ***tri-state bus***.

19.5.4. Bargh as modified by Schubert does not specifically teach displaying the instrumentation data relating to the ***tri-state bus*** in response to the query.

19.6. Koseko appears to teach a logic design that includes a tri-state bus (***Page 512, section 1 Introduction, and figure 1***).

19.7. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Koseko with the art of Bargh as modified by Schubert to produce the claimed invention.

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20. Claims 26 - 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bargh as applied to claim 25 above, in view of Watkins (U.S. Patent 5,220,512).

20.1. Bargh teaches an apparatus of a logic design element that automatically collects instrumentation data as recited in claim 25 above.

20.2. Regarding claim 26:

20.2.1. Bargh does not specifically teach:

20.2.1.1. a display module that is structured and arranged to display the instrumentation data relating to the logic element design

20.2.2. Watkins appears to teach:

20.2.2.1. a display module that is structured and arranged to display the instrumentation data relating to the logic element design (***column 7, lines 12 – 19; and figure 3; and figure 2, element 224***).

20.2.2.1.1. Regarding (***column 7, lines 12 – 19; and figure 3; and figure 2, element 224***); Column 7, lines 12 – 19, recites that the simulation module

displays the instrumentation data; therefore the logic simulator (***figure 2, element 224***) is a display module.

20.2.3. The motivation to use the art of Watkins with the art of Bargh would have been the benefit recited in Watkins that it is possible for the user to indicate that only certain components are to be compiled and simulated, thus improving the compile and simulation times (column 6, lines 60 – 65).

20.2.4. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Watkins with the art of Bargh to produce the claimed invention.

20.3. Regarding claim 27:

20.3.1. Bargh does not specifically teach:

20.3.1.1. an interface module that is structured and arranged to receive a query to display the instrumentation data relating to the design element, wherein the display module is structured and arranged to display the instrumentation data relating to the logic design element in response to the query.

20.3.2. Watkins appears to teach:

20.3.2.1. an interface module that is structured and arranged to receive a query to display the instrumentation data relating to the design element, wherein the display module is structured and arranged to display the instrumentation data relating to the logic design element in response to the query (***column 6, lines 45 – 53***).

20.3.2.1.1. Regarding (***column 6, lines 45 – 53***); attaching a data area that displays state data is a query. Watkins teaches software to receive a query, therefore it is inherent that there is a portion of code that receives the query, which is an interface module to receive the query.

21. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bargh as applied to claim 25 above, in view of Srivastava (Mani B. Srivastava et al; "Using VHDL for High-Level, Mixed –Mode System Simulation", September 1992, IEEE Design & Test of Computers, Volume 9, Issue 3).

21.1. Bargh teaches an apparatus of a logic design element that automatically collects instrumentation data as recited in claim 25 above.

21.2. Claim 28 is a dependent claim of claim 25, and thereby inherits all of the rejected limitations of claim 25.

21.3. The art of Srivastava is directed to logic simulation (**Title**).

21.4. Regarding claim 28:

21.4.1. Bargh appears to teach that the collection module is integrated with the logic design element and is structured and arranged to automatically collect the instrumentation data relating to the logic element during the simulation (***figure 4B, element 420; and column 12, lines 25 – 67, and columns 13 – 14***).

21.4.2. Bargh does not specifically teach that the collection module is integrated with the ***FIFO memory*** and is structured and arranged to automatically collect the instrumentation data relating to the ***FIFO memory*** during the simulation.

21.4.3. Srivastava appears to teach that the logic design element includes a FIFO memory (***page 36, figure 3, message buffer***).

21.4.4. The motivation to use the art of Srivastava with the art of Bargh is the advantages recited in Srivastava that VHDL enables simulation across many different levels of abstraction (***page 31, last sentence, and page 32, first two sentences***). This advantage would have been recognized by the ordinary artisan as a benefit.

21.4.5. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Srivastava with the art of Bargh to produce the claimed invention.

22. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bargh as applied to claim 25 above, in view of Koseko (Yasushi Koseko; "Tri-state bus conflict checking method for ATPG using BDD", 1993, Proceedings of the 1993 IEEE/ACM International conference on Computer-aided design, pages 512-515).

22.1. Bargh teaches an apparatus of a logic design element that automatically collects instrumentation data as recited in claim 25 above.

22.2. Claim 29 is a dependent claim of claim 25, and thereby inherits all of the rejected limitations of claim 25.

22.3. The art of Koseko is directed toward tri-state bus conflict checking (***Title***).

22.4. Regarding claim 29:

22.4.1. Bargh appears to teach that the collection module is integrated with the logic element and is structured and arranged to automatically collect the

instrumentation data relating to the logic element during the simulation (***figure 4B, element 420; and column 12, lines 25 – 67, and columns 13 – 14***).

22.4.2. Bargh does not specifically teach that ***the logic design element includes a tri-state bus***.

22.4.3. Bargh does not specifically teach that the collection module is integrated with the ***tri-state bus*** and is structured and arranged to automatically collect the instrumentation data relating to the ***tri-state bus*** during the simulation.

22.4.4. Koseko appears to teach that a logic design element includes a tri-state bus (***Page 512, section 1 Introduction, and figure 1***).

22.4.5. Koseko appears to teach collecting the instrumentation data relating to the ***tri-state bus*** during the simulation (**page 515, table 1**).

22.4.6. The motivation to use the art of Koseko with the art of Bargh is the benefit recited in Koseko that the method is a practical bus design rule checking method that avoids wasteful work avoids wasteful work (**page 512, section 1. Introduction, right-side column, third paragraph**).

22.4.7. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Koseko with the art of Bargh to produce the claimed invention.

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23. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bargh as modified by Schubert as applied to claims 1 - 2 and 13 above, further in view of Srivastava (Mani B.

Srivastava et al; "Using VHDL for High-Level, Mixed –Mode System Simulation", September 1992, IEEE Design & Test of Computers, Volume 9, Issue 3).

23.1. Bargh as modified by Schubert teaches a method of simulating a logic design as recited in claims 1 - 2 and 13 above.

23.2. Regarding **claim 32**:

23.3. Bargh as modified by Schubert does not specifically teach:

23.3.1. the logic design element represents a FIFO memory;

23.3.2. the instrumentation data collected by the logic design element comprises statistics regarding usage of the FIFO memory.

23.4. Srivastava appears to teach:

23.4.1. the logic design element represents a FIFO memory (***page 36, figure 3, message buffer***).

23.4.2. the instrumentation data collected by the logic design element comprises statistics regarding usage of the FIFO memory (***page 36, figure 3, message buffer and statistics***).

23.5. The motivation to use the art of Srivastava with the art of Bargh is the advantages recited in Srivastava that VHDL enables simulation across many different levels of abstraction (***page 31, last sentence, and page 32, first two sentences***). This advantage would have been recognized by the ordinary artisan as a benefit.

24. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Srivastava with the art of Bargh to produce the claimed invention.

25. Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the Applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Allowable Subject Matter

26. Claims 30 - 31 and 33 – 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure

27.1. Beardslee (U.S. Patent Number 7,072,818) teaches a collection module that is integrated with a logic design element to collect and store instrumentation data representing usage and performance statistics;

27.2. Sumner (U.S. Patent Application Publication 2002/0184615) teaches inserting code into a computer program to collect statistics.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday – Friday 9:00 AM – 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

8/18/05